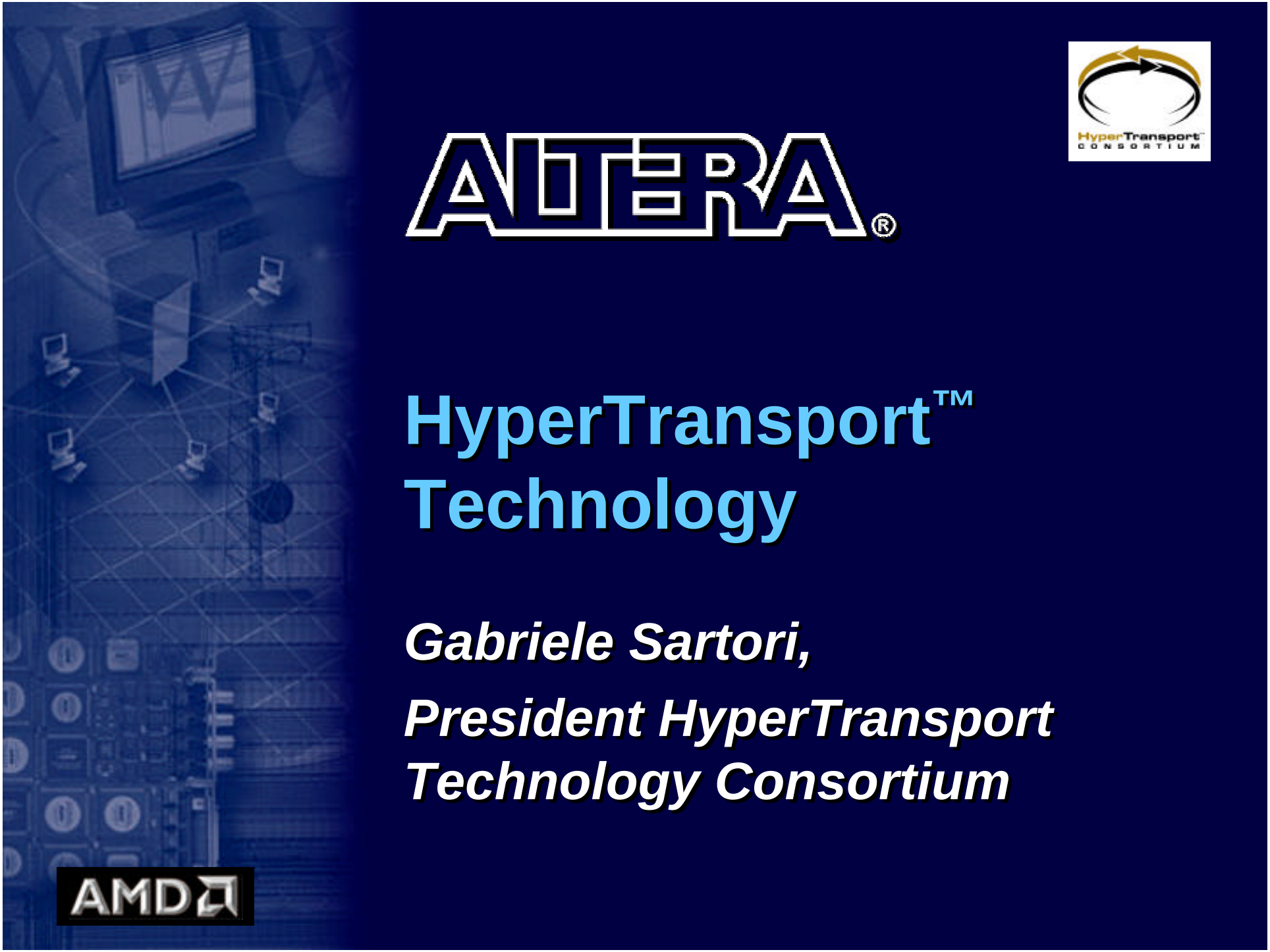
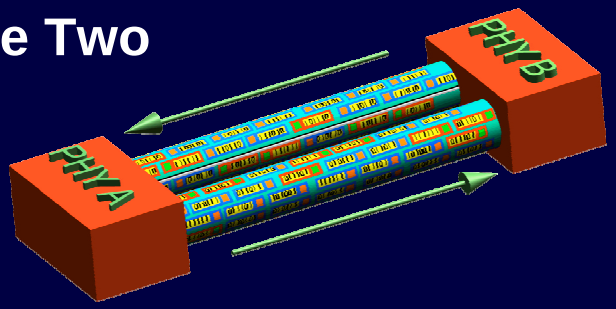


HyperTransport™ Technology

Gabriele Sartori,

President HyperTransport Technology Consortium

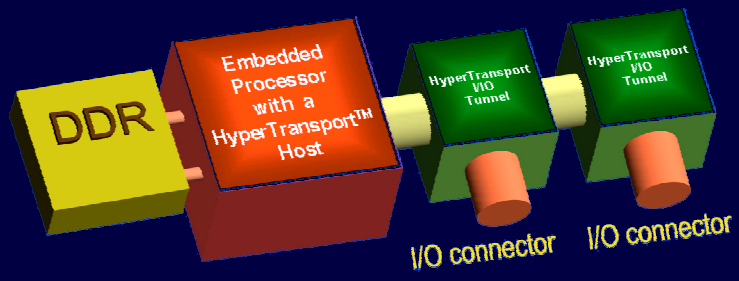
HyperTransport Technology Basics



- HyperTransport Technology Buses Have Two Unidirectional Point-to-Point Links
  - The Links Can Be 2-, 4-, 8-, 16- or 32-Bits Wide in Each Direction
  - HyperTransport Links Have Data Rate up to 1600 Mbps per Pin-Pair (800 MHz Clock)
    - e.g., 4 Bits Each Way Give up to 1.6 Gbps Total Bandwidth
    - e.g., 8 Bits Each Way Give up to 3.2 Gbps Total Bandwidth
    - e.g., 16 Bits Each Way Give up to 6.4 Gbps Total Bandwidth
    - e.g., 32 Bits Each Way Give up to 12.8 Gbps Total Bandwidth
- Packets are Multiples of 4 bytes in Length
- Serial Link with Commands, Addresses & Data Use Same Bits

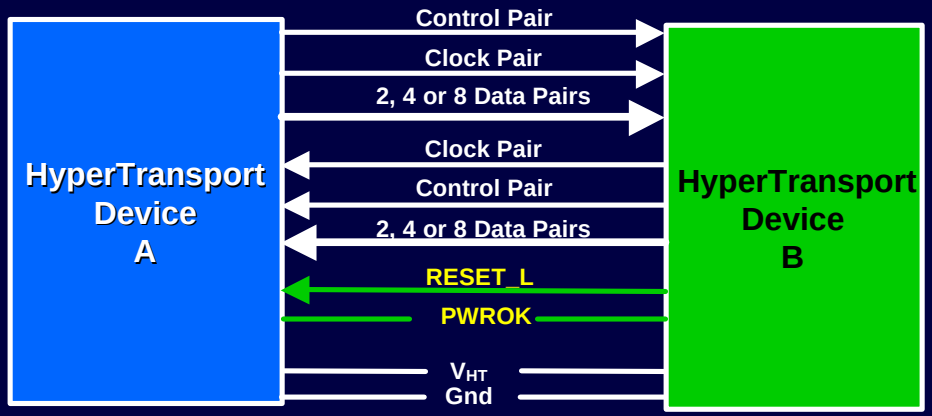
Embedded Applications & I/O Tunnels

- First Time in the Industry
  - I/O Devices Shared among Computation & Communication Industry
  - Unique “TUNNELING” Capability Gives Almost Unlimited I/O Expandability
  - Fundamentally Different Microprocessor & Memory Controllers May Be Designed to Use the Same I/O Components
  - Pin Count Adjustable for Necessary Bandwidth
  - Cost Reduced Due to Cumulative Volume
  - Extended Component Life



HyperTransport Device Pin Count

- Additional HyperTransport Device Signals
  - Power OK (PWROK)
  - Reset HyperTransport Device (RESET_L)
- 55-pin HyperTransport Device Bus Provides 12X the Bandwidth of PCI-32/33 with Fewer Pins
- Signal to Ground Ratio Is Designed to Be 4:1
- Optional Link Power Down Signals for Mobile Systems
  - HyperTransport Device Stop_l
  - Devreq_l
- Power Per Pin-pair Is Nil When in HyperTransport Device Stop Mode



Bus Width (Each Way)	2	4	8	16	32
Data Pins (total)	8	16	32	64	128
Clock Pins (total)	4	4	4	8	16
Control Pins (total)	4	4	4	4	4
Subtotal (high speed)	**16**	**24**	**40**	**76**	**148**
VLDT	2	2	3	6	10
GND	4	6	10	19	37
PWROK	1	1	1	1	1
RESET_L	1	1	1	1	1
Total Pins	**24**	**34**	**55**	**103**	**197**
Total Max BW GB/s	**0.8**	**1.6**	**3.2**	**6.4**	**12.8**

DC Power per Pin-Pair: 4 - 9 mW, 6 mW$_{Typical}$
Signal to V_{HT}/Gnd Ratio: 4:1

Applications for HyperTransport Technology

- Routers
- Hubs
- Switches
- Servers
- Workstations
- PCs (Desktop & Notebook)
- Set-Top Boxes
- Mobile/Handheld Devices
- Game Consoles
- Embedded Systems

Any Application Requiring High Speed, Low Latency & Scalability!

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HyperTransport Technology Milestones

- First Public Presentation on HyperTransport Technology Microprocessor Forum 1999
- Operational Specification Version 1.0 Finished May 2000 AMD Distributes under NDA
- HyperTransport Technology Presentation with Technical Information at Winhec 2000
- HyperTransport Technology White Paper Available Early 2000 through AMD
- HyperTransport Technology Presentation at Platform 2000 (June 2000)
- 100+ Companies Evaluating Specification & Several Licensing Technologies through AMD (2000)
- HyperTransport Technology Consortium Officially Launched July 24, 2001

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HyperTransport Technology Milestones

- First HyperTransport Technology-Based South Bridge Announced by NVIDIA (June 2001)
- Sibyte (Broadcom) Announced Its MIPS CPU with HyperTransport Technology
- Sandcraft Announced Its HyperTransport Technology Roadmap
- Altera First PLD Family Supporting HyperTransport Technology in Q1 2001
- Teradyne & Dolphin Technology Announce First Test Equipment for HyperTransport Technology (May 2001)
- Multiple HyperTransport Technology-Based Chipsets for AMD Athlon™ Processors in 2001
- HyperTransport Technology-Based Products Planned from AMD in 2002

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HyperTransport Technology Consortium

- Incorporated As Non-Profit Corporation & Officially Announced 7/24/2001
- Manages & Controls Development & Evolution of the Specification
- Widespread Support Planned in Networking, Telecommunications, Computers & Embedded System Companies
- Members Have Access to Technical Specifications & May Participate in Consortium Meetings & Events
- Two Membership Levels Available: Contributor & Adopter
- To Become Member, Visit www.hypertransport.Org
- Charter Members Comprise Executive Committee & Include:

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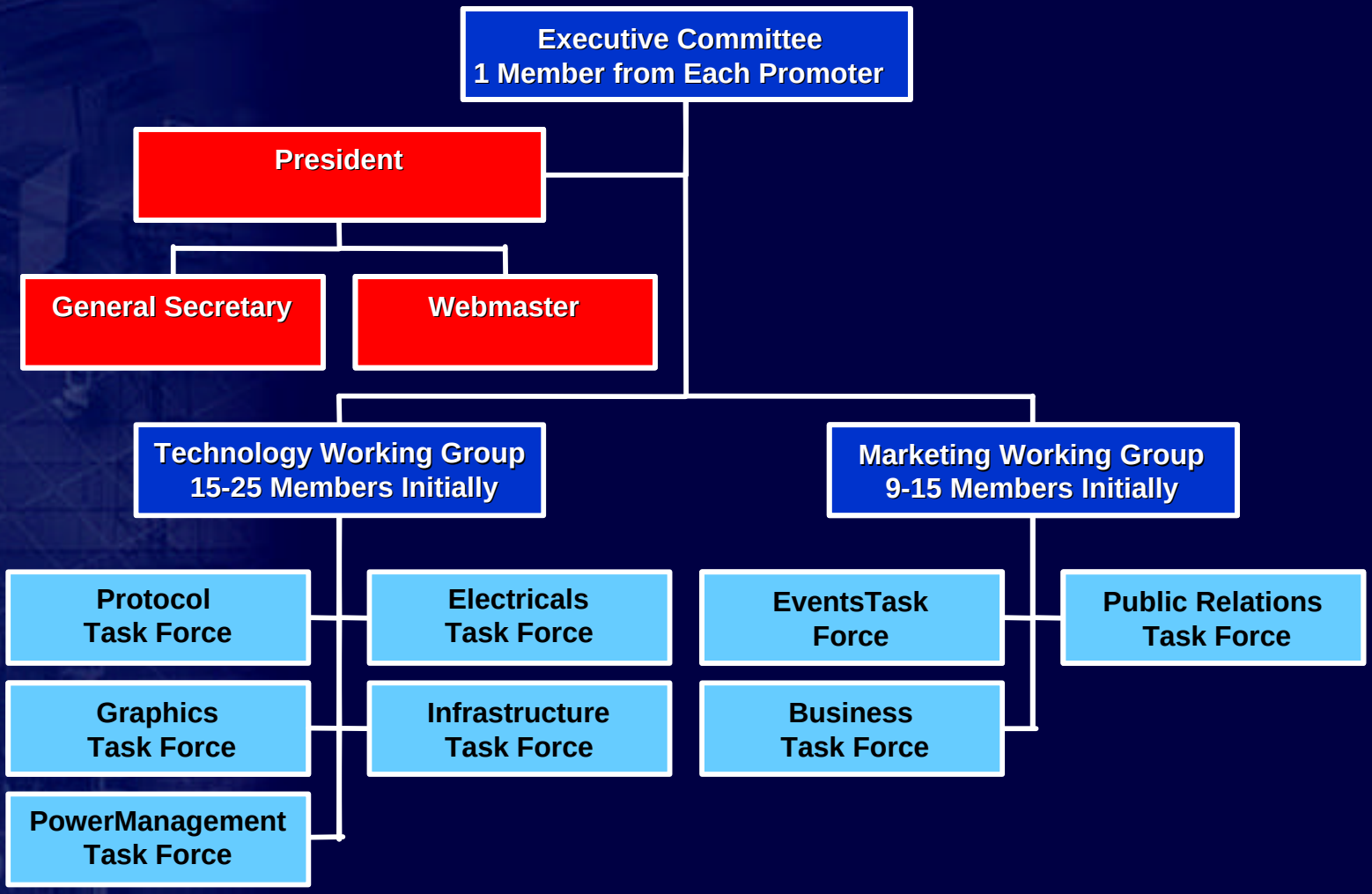
Consortium Structure



Summary

- HyperTransport Technology Is an Innovative Technology Designed to Enable Chips Inside of PCs, Networking & Communications Devices Like Those that Power the Internet, to Communicate with Each Other up to 24 Times Faster than Existing Technologies
- Newly Formed HyperTransport Technology Consortium Is Helping to Drive HyperTransport Technology to Market
  - Consortium Incorporated & Announced July 24, 2001
  - Industry Heavyweights Comprise Consortium's Executive Committee – AMD, API Networks, Apple Computer, Cisco Systems, NVidia, PMC-Sierra, Sun Microsystems, Transmeta
- Consortium Members Announce Products Using HyperTransport Technology Are Planned to Ship Later in 2001

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